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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,024	09/05/2003	Gun-Ok Jung	2557-000170/US	6042
30593	7590	04/18/2006	EXAMINER	
HARNESS, DICKEY & PIERCE, P.L.C.				COX, CASSANDRA F
P.O. BOX 8910		ART UNIT		PAPER NUMBER
RESTON, VA 20195		2816		

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/655,024	JUNG ET AL.	
<b>Examiner</b>	<b>Art Unit</b>		
Cassandra Cox	2816		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 30 January 2006.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-21 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 9-13 and 21 is/are allowed.  
 6) Claim(s) 1,8,14 and 15 is/are rejected.  
 7) Claim(s) 2-7 and 16-20 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 05 September 2003 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1.) Certified copies of the priority documents have been received.  
 2.) Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3.) Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
     Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
     Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_

## DETAILED ACTION

Applicant's arguments filed September 21, 2005 have been fully considered but they are not persuasive. The previous rejection is repeated below. In addition the newly added limitation has been rejected using the same art in the previous rejection.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 8, and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Takaya (U.S. Patent No. 5,783,967).

In reference to claim 1, Takaya discloses in Figure 2 a frequency multiplier comprising a delay circuit (22) that receives a first clock signal (21) having a first frequency and outputs a delayed clock signal, the delay circuit (22) producing the delayed clock signal by applying a time delay to the first clock signal (21); an XOR gate (26) that receives the first clock signal (21) and the delayed clock signal (output of delay block 22), performs an XOR operation on the first clock signal (21) and the delayed clock signal, and outputs a second clock signal (OUTPUT); a control circuit (23, 24, 25) that detects a phase difference between the first clock signal (21) and the delayed clock signal, and outputs a control signal to the delay circuit (22) corresponding to the detected phase difference, wherein the control signal controls a duration of the time delay applied to the first clock signal (21) by the delay circuit (22), the control signal is

increased or decreased in response to a logic signal (see Figure 4 which shows the phase comparator 24 and loop filter 25 of Figure 2, the control signal (DELAY CONTROL VOLTAGE OUTPUT) is increased or decreased in response to a logic signal (the logic signal is the signal controlling the gates of the pull up and pull down transistors shown in Figure 4), the output is increased when the pull up transistor is turned on in response to the logic signal at its gate and the output is decreased when the pull down transistor is turned on in response to the logic signal at its gate). The same applies to claims 14 and 15.

In reference to claim 8, Takaya discloses that the second clock signal (OUTPUT) would have a second frequency that is twice that of the first frequency (INPUT), see column 3, lines 40-50.

### ***Response to Arguments***

3. Applicant's arguments filed September 21, 2005 have been fully considered but they are not persuasive. Applicant's argument that Takaya does not disclose "increasing or decreasing in response to a logic signal" is not persuasive. Takaya discloses in Figure 4 the phase comparator 24 and loop filter 25 of Figure 2. The control signal (DELAY CONTROL VOLTAGE OUTPUT) is increased or decreased in response to a logic signal (the logic signal is the signal controlling the gates of the pull up and pull down transistors shown in Figure 4), the output is increased when the pull up transistor is turned on in response to the logic signal applied at its gate and the output is decreased when the pull down transistor is turned on in response to the logic signal

applied at its gate). While applicant's argument's seem to focus on signal V1 being increased or decreased in response to CLK1 and CLKD, it is the examiner's interpretation of the claims (based on review of the specification and drawings) that the control circuit refers to block 230 as a whole and the control signal refers to the signal (CTRL) being increased or decreased in response to the logic signal generated by the comparator 232. Takaya's circuit disclosed in Figures 2 and 4 is capable of increasing or decreasing its control signal in response to a logic signal (see rejection above).

***Allowable Subject Matter***

4. Claims 9-13 and 21 are allowed.
5. Claims 2-7, and 16-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. The following is a statement of reasons for the indication of allowable subject matter: Claims 2, 6-7, and 20 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the control signal (CTRL) includes a plurality of bit signals corresponding to the detected phase difference, each bit signal having a logic state in combination with the rest of the limitations of the base claims and any intervening claims. Claims 3-5 and 16-19 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the control circuit includes a comparator (232) and a counter (233) in combination with the rest of the limitations of the base claims and any intervening claims.

Art Unit: 2816

7. The following is an examiner's statement of reasons for allowance: Claims 9-13 and 21 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the control circuit includes a comparator (232) and a counter (233) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2816

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC  
*Cassandra Cox*

April 11, 2006